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Journal of Low Power Electronics

Special Issue on Power, Parasitics, and Process-Variation (P3) Awareness in Mixed-Signal Design

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Modern consumer electronic systems which have profound effect on society are Analog/Mixed Signal Systems-On-Chip (AMS-SoCs). The aim of this special issue is to cover design techniques and computer-aided design (CAD) techniques that incorporate power, parasitics, and process-variation (P3) awareness in these AMS-SoCs. Power dissipation has significant impact on every aspect of the AMS-SoCs. Acceptability, reliability, and profitability of these AMS-SoCs depend as much on power efficiency as on performance. Another issue of the AMS-SoC design is that the exact performance prediction is very challenging due to large parasitic (RLCK) effects. Unfortunately, it is difficult to estimate the parasitic effects before the circuit is implemented. Therefore, to improve design efficiency and reduce time-to-market, it is crucial to be able to predict parasitic effects for accurate performance and then integrate techniques to compensate the effects. The design cycle of the AMS-SoCs is complicated by the impact of process variation due to the use of state-of-the-art nanoscale technologies for fabrication. The process point, which is the center of the distribution of the process-parameters, may not be the best design point to maximizing yield. Therefore AMS-SoCs need to be designed to perform across the entire process and operating environment to enhance the yield. Thus, the topics of interest within the scope of this special issue include, but are not limited to, the following areas:

- Methodologies for fast AMS-SoC design space exploration.
- Static low-power design techniques for analog/mixed-signal circuits and systems.
- Dynamic power-management techniques for analog/mixed-signal circuits and systems.
- Techniques to model RLCK parasitics for AMS-SoC design space exploration.
- Static techniques to compensate effects of RLCK parasitics in AMS-SoC.
- Circuit and system level process-variation impact analysis techniques for AMS-SoC.
- Static design-time techniques for process-variation impact compensation in AMS-SoC.
- Dynamic post-silicon process-variation compensation techniques for AMS-SoC.
- CAD algorithms, flows, and methodologies for P3-Awareness in AMS-SoC.
- AMS-SoC design and CAD using post-nano-CMOS technology like carbon nanotube (CNT) and double-gate FET (DGFET).
- Application specific AMS-SoC case studies.

Authors are invited to submit original unpublished articles as a single PDF file as an email attachment to saraju.mohanty@unt.edu. Please refer to http://www.aspbs.com/jolpe/ for manuscripts formatting guidelines. The articles will be selected for publication through the peer review process. All correspondence regarding this special issue should be addressed to the Guest Editor, Prof. Saraju P. Mohanty, Dept. of Computer Science and Engineering, University of North Texas, Denton, TX 76203. Email: saraju.mohanty@unt.edu.

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