

## Journal of Low Power Electronics

*Special Issue on Low Power Design and Verification Techniques*

**Guest Editor**  
**Shireesh Verma**  
[shireesh@ieee.org](mailto:shireesh@ieee.org)

**Editor-In-Chief**  
**Patrick Girard**  
[patrick.girard@lirmm.fr](mailto:patrick.girard@lirmm.fr)

Power consumption has become a critical benchmark for semiconductor devices in shrinking nano-geometries. Voltage based techniques like Power Domains, Power and Clock Gating, State Retention, Isolation, Multiple Supply Voltages, Dynamic Voltage Scaling, Adaptive Voltage Scaling, Active Body Bias, etc. are predominantly used for managing chip power consumption. The use of such techniques has significant impact on the chip architecture as well as micro-architecture. They introduce additional complexity to the design state space as well as test circuitry, which translates to an aggravated verification challenge. Traditional HDL simulators are not equipped to simulate the multiple and variable power supplies, and the higher abstraction level of the RTL does not allow simulation of some of the power management techniques. As a result, a specialized set of design and verification tools is needed to ensure silicon success. The topics of interest within the scope of this special issue include, but are not limited to, the following areas:

- *Power management architectures and exploration*
- *Design techniques and algorithms*
- *Verification techniques and algorithms*
- *Design and Verification Tools*
- *Power intent capture and standards (e.g. IEEE P1801)*
- *Multi voltage and domain simulation techniques*
- *Modeling and verification of circuit level behavior at RTL abstraction level*
- *Formal and Dynamic verification of power sequencing protocols*
- *Power management implications on testability*
- *Manufacture technology specific considerations*
- *Application specific case studies*

Authors should submit original unpublished research articles as a PDF file as an attachment in an email to [shireesh@ieee.org](mailto:shireesh@ieee.org). The submissions should be complete and publication ready in all details. Please refer to <http://www.aspbs.com/jolpe/> for instructions, style and formatting guidelines. The articles will be selected for publication through the journal's peer review process.

All correspondence regarding this special issue should be addressed to the Guest Editor, **Dr. Shireesh Verma**, Conexant Systems Inc., 4000 MacArthur Blvd., Newport Beach, CA 92660. Ph: +1 (949) 483 5741, Email: [shireesh@ieee.org](mailto:shireesh@ieee.org)

### **Timeline:**

Manuscript Submission Deadline: **July 15, 2010**  
Notification: **October 31, 2010**  
Final Manuscript Submission Deadline: **November 30, 2010**  
Tentative Publication Date: **February, 2011**

